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13. ABSTRACT *(Maximum 200 words)*

The goal of this program was to develop ultra-fast superconducting digital technology based on HTS Josephson junctions on silicon substrates. Working Josephson junctions and SQUID's were successfully fabricated on silicon, and an Yttrium-Barium-Copper-Oxide RSFQ rs flip-flop with 14 junctions and I/O test structures was successfully designed, fabricated, and tested. The kinetic inductance and London penetration depth of the films on silicon were determined from measurements of SQUIDs on silicon. Minimizing kinetic inductance through the use of thicker films will be required in future devices. An approach to alleviating film stress in these thicker films due to thermal expansion coefficient mismatch is outlined. This proposed solution involves fabricating a functionally graded buffer layer that can flow plastically to relieve stress while at the same time, allows nucleation and growth of heteroepitaxial films. A wafer bonding facility was constructed and utilized to demonstrate the successful bonding of silicon and BPSG coated wafers, a key step in the compliant substrate fabrication procedure.

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PHASE I
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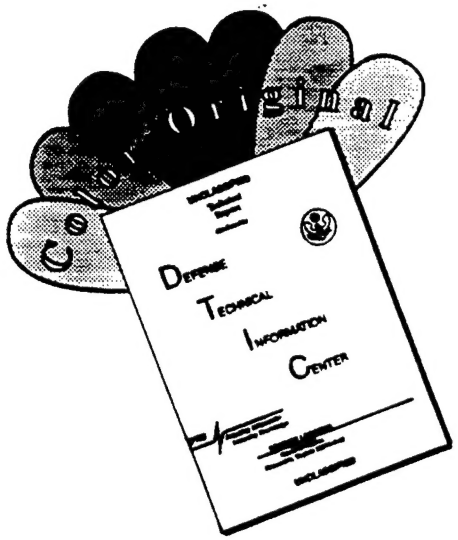

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I.1. Introduction

I.1.1. The Problem

Manufacturable High Temperature Superconducting Digital Electronics - Superconducting electronics have long been regarded as having the potential for superior switching speeds and reduced power consumption compared to semiconducting device families, however, the requirement for refrigeration to temperatures near 4.2 K has been a major stumbling block to the commercialization of low T_c superconducting logic. High temperature superconducting (HTS) materials present new opportunities for superconducting electronics.

At present there are very few Josephson HTS technologies which can be considered for applications requiring a non-trivial number of high quality junctions. Among these are SNS junctions, where N may be a noble metal[1] or a conductor compatible with HTS materials[2], bi-epitaxial junctions[3], and e-beam written junctions.[4] It is fair to say that none of the existing HTS Josephson technologies have fully matured, and much additional work is required to make them useful in applications. Because many targeted applications of superconducting electronics rely on the high switching speeds attainable by Josephson junctions, rf properties have played a significant role in the search for practical substrates.

Silicon, quartz, sapphire and glass substrates are attractive substrates for HTS device technology due to their:

- Large size availability and low cost
- Superior dielectric, thermal conduction, and strength properties compared to MgO or the perovskite related substrate materials.
- Compatibility with both VLSI silicon and HTS materials technologies through various wafer bonding or ion-implantation fabrication procedures.
- Extensive preexisting technology base.
- Transparency from mid-infrared to microwave frequencies (at cryogenic temperatures)[5]

I.1.2. The Opportunity

HTS digital josephson technology for silicon and other rf compatible substrates- A method for growing epitaxial thin films of $Y_1Ba_2Cu_3O_7$ (YBCO) on silicon substrates and the demonstration of YBCO Josephson junctions on silicon during this Phase I program bring the possibilities of practical manufacturable, high performance superconducting electronics closer to reality. The adoption of silicon as a substrate material raises the tantalizing possibility of a monolithically integrated technology, combining the speed and power consumption of superconducting electronics with the tremendous benefits offered by modern VLSI silicon technology. In addition to novel hybrid applications involving integrated semiconducting and superconducting components, a Josephson technology fully compatible with silicon substrates would find broad acceptance for most of the classic applications of the Josephson effects[6] including Superconducting Quantum Interference Devices (SQUIDs), Josephson array oscillators, infrared detectors, Josephson mixers and heterodyne receivers, digital logic, A to D converters, and millimeter/submillimeter-wave spectrum analyzers.

Developments in wafer bonding and etchback raise the additional possibility of developing a YBCO technology for silicon, quartz or glass substrates with greatly reduced stress due to thermal expansion mismatch during growth and cooldown. Applying these techniques could greatly improve the performance of many rf components such as filters, delay lines and receivers as well as high speed active Josephson components.

I.2. Summary of Phase I

Phase I was performed in three tasks with the following objectives:

Task 1. - Josephson Junction Fabrication and Testing: To verify the junction fabrication process on silicon substrates, and to produce a set of junctions for electrical and statistical testing.
Task 2. - RSFQ Logic Modeling and Design: To design and simulate RSFQ circuit elements that can be successfully fabricated and tested.
Task 3. - RSFQ Circuit Fabrication and Testing: To fabricate working HTS RSFQ logic elements on silicon substrates.

The junction technology developed in Phase I was based on the electron beam modification technique. To summarize briefly, thin Ytrria stabilized zirconia (YSZ) buffered HTS films were deposited on silicon substrates, and patterned into narrow ~4 μm wide bridges. These bridges were then written over by a narrow (~5 nm width) electron beam of high energy. The electron beam has the effect of "damaging" the HTS material over a length comparable to the coherence length, forming a Josephson junction. The electron beam writing process is believed to be associated with the formation of displaced-oxygen/vacancy pairs in the crystal structure that locally disrupt the superconductivity.

The highlights of the Phase I accomplishments include:

Working Josephson junctions and SQUIDs have been fabricated on silicon substrates. The electrical properties are similar to those fabricated on more conventional substrates such as $LaAlO_3$.

A YBCO RSFQ rs flip flop with 14 junctions and I/O test structures was successfully designed, fabricated and tested.

The kinetic inductance and London penetration depth of the films on silicon have been determined from measurements of HTS SQUIDs on silicon.

An approach to alleviating film stress due to thermal expansion coefficient mismatch has been outlined. The proposed solution involves fabricating a functionally graded buffer layer that flows plastically to relieve film stress while at the same time, allows nucleation and growth of heteroepitaxial films.

A wafer bonding facility was constructed at AFR and utilized to demonstrate the successful bonding of silicon and BPSG coated wafers, a key step in the compliant substrate fabrication procedure.

I.3. Conclusions

The quality of the junctions in the exploratory Phase I program was sufficient to fabricate complex HTS devices based on these junctions. However, several factors associated with the use of silicon as a substrate emerged as technical barriers. HTS film thickness was identified as a particularly important factor. It is necessary to minimize parasitic inductance in order to achieve high quality HTS RSFQ circuits, and to do this thicker films will be required. The maximum crack-free YBCO film thickness on YSZ-buffered silicon seems to be about 70 nm. The 25 nm films used in Phase I were adequate for forming good junctions, as determined by the measurements of Shapiro steps, and the magnetic modulation, but this is not good enough for complex circuits. To obtain the required thicker films, without cracking, we have devised methods to use a compliant buffer layer on the silicon substrates. This buffer layer, of a plastically deformable glass, would relieve the stress due to differential thermal expansion between the silicon wafer and the YBCO, potentially allowing thick (>500 nm) crack-free YBCO films. We have proposed in Phase II to pursue development of the deformable buffer layer and e-beam junction technology to achieve stable, reproducible fabrication of devices using the ultra-fast RSFQ logic family.

II. Detailed Results and Discussion

For completeness, the background section from the Phase I proposal is repeated here.

II.1. Background From Phase I Proposal

The backround of the proposal is in three areas: i) HTS Josephson junction technology, ii) the RSFQ logic family, and iii) HTS thin film fabrication on silicon substrates.

II.1.1. HTS Josephson Junction Technology

Josephson junctions are the building blocks of any superconducting digital switching circuit. While a low-T_c niobium technology has a choice between hysteretic and nonhysteretic (latching - nonlatching) Josephson elements, the HTS technology is limited to nonhysteretic elements. This in turn dictates a choice of logic implementations, with Rapid Single Flux Quantum (RSFQ) logic at the top of the list in terms of concept maturity, proven low -T_c performance and its potential for ultra-high data throughput.[7] In this context, the nonhysteretic nature of HTS junctions is not a limitation; in fact quite the opposite[7]. With low -T_c junctions, the main challenge faced by this new digital technology is helium refrigeration which is unacceptable for many potential users. Transfer to HTS circuits operating at temperatures above 20 - 30 K would go a long way toward the acceptance of this technology.

Electron beam modified junctions

Electron beam writing method - The method developed at Stony Brook consists of direct writing of Josephson weak links on prepatterned HTS thin-film microbridges by a focused electron beam[4]. In the present Stony Brook junctions, 25 nm and 50 nm $c_{\perp}$-oriented YBCO films, grown by the BaF_2 process[8] on $LaAlO_3$ substrates, are patterned into 2-3 μm wide and 4 μm long bridges using standard photolithography with PMMA resist and Br-methanol etching. A 1.5 nm electron beam of a Philips CM-12 electron microscope with energy ranging from 20 keV to 120 keV and beam current 0.6 nA at 120 keV is scanned once across the microbridge, stopping at 2048 equidistant points, about 2 nm center- to-center, for a preset dwell time between 0.1 s and 2 s. Preliminary studies using a much higher beam current of about 10 nA, a 10 nm spot size and shorter dwell time suggests that the junction quality is as good as with the small spot size and longer dwell time. It is likely that the writing speed of the Philips CM-12 microscope can be increased to about 2 μm/min., i.e. one junction per minute, which will allow the fabrication of multi-junction circuits of reasonably high complexity. Thus produced junctions can be studied and utilized in circuits either as made , after e-beam writing, or, more commonly, after a mild stabilizing annealing at 330 K- 360 K. The purpose of this annealing is to slow down the drift of the junction parameters at room temperature, and to adjust junction T_c and operating temperature to a desired level.

Junction properties

Critical temperature - One of the big advantages of e-beam writing technology is that the most important junction parameters such as T_c, I_c, and, to a lesser degree, R_n can be tuned to the desired values simply by changing the irradiation dose given to the junction or by adjusting the parameters of a subsequent stabilizing anealing. For example, the T_cs from a few degrees K to 88 K can be obtained. The best operating temperature for the e-beam junctions is of the order of (0.9-0.95) T_c (see below). An ability to change T_c implies an ability to choose the operating temperature. This is important if one needs to adjust the operating temperature as may be dictated by design considerations, such as circuit tolerance to the digital error rates.

We further note that the T_c vs. dose dependence shows a pronounced 60 K plateau, which is qualitatively similar to the well known T_c vs. oxygen content dependence in YBCO. This is especially beneficial for reproducible junction fabrication due to a weak dose dependence in the plateau region.

Current - voltage characteristics - At critical current densities J_c up to $2\times10^5 A/cm^2$, or I_c up to 0.2 mA in 2 μm wide and 50 nm thick bridges, the junctions are perfectly described by the RSJ model with thermal noise (see Figure 1). At higher j_c there is a transition to flux flow I-V characteristics which can be attributed to the transition from short ($w<\lambda_J$) to long ($w>\lambda_J$) junction behavior. Temperature dependences of I_c and normal resistance R_n can be inferred from the RSJ fit. Figure 2 shows j_c as a function of reduced temperature T/T_c for junctions with different T_c's. The last point on each curve roughly corresponds to the boundary of the RSJ behavior. At 77 K the I_cR_n product for e-beam junctions is in the range of 0.2 mV - 0.4 mV.

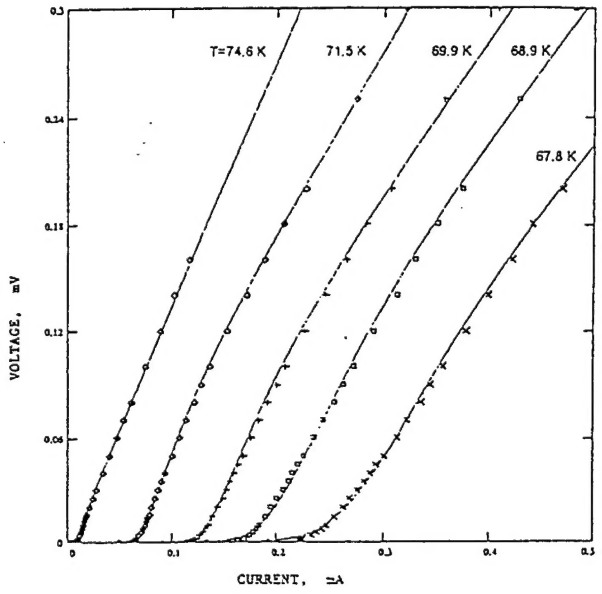

Figure 1 Current-Voltage characteristics of e-beam junctions at different temperatures. Lines indicate fits to RSJ model with fluctuations

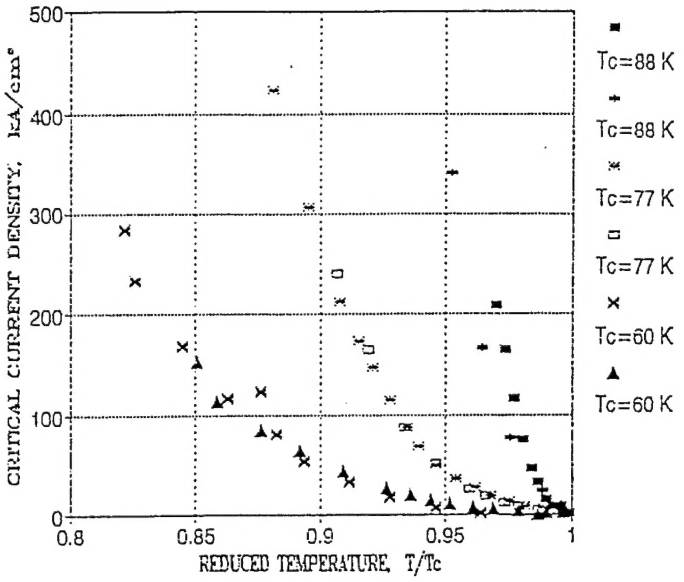

Figure 2 Temperature dependences of the critical current density of e-beam junctions with different critical temperatures..

Electromagnetic properties - It is well known that the magnetic field modulation of the Josephson critical current serves as a fine characteristic of the junction uniformity, which in turn implies good noise characteristics. Perfect magnetic field modulation can seldom be seen in the literature on HTS junctions. The e-beam writing technology has great potential in this respect. For j_c in the RSJ range (see Figure 2 and the discussion in the previous paragraph,) the magnetic field modulation of the critical current for our junctions is almost perfect (see Figure 3). At higher critical current densities, the modulation is not complete since the junctions are in the long junction regime.

Under microwave irradiation, the e-beam junctions show oscillations of the critical current with microwave power according to the RSJ model and Shapiro steps to high order (Figure 4), once again indicating the high quality of the e-beam junctions. The measurements of junction noise we are currently performing show that the high frequency noise is of purely thermal nature. Low frequency (1Hz - 10 Hz) noise of our junctions at 77 K shows the usual 1/f component and is also low compared to most HTS junctions.

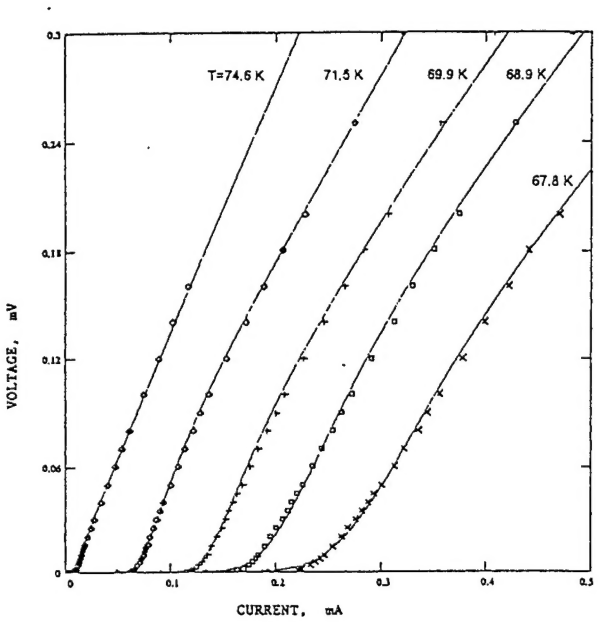

Figure 3 Magnetic field modulation of the critical current.

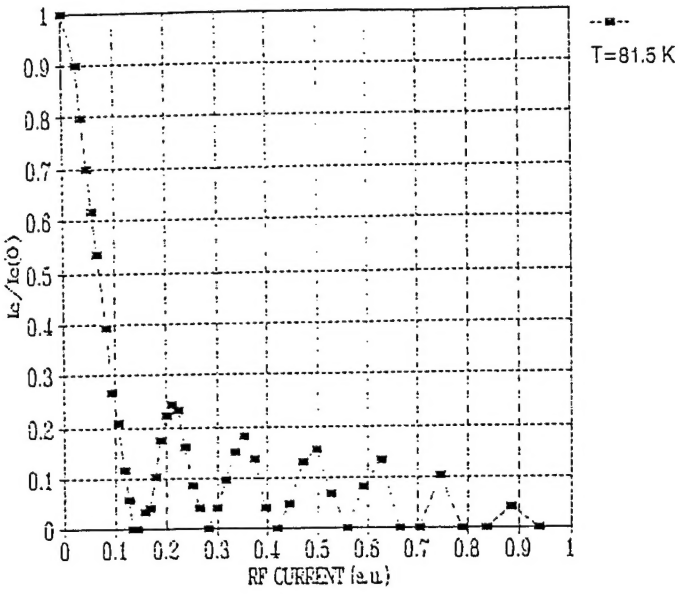

Figure 4 Oscillations of the Josephson critical current in a 10 GHz microwave field.

We conclude that the e-beam writing technology enables fabrication of high quality HTS Josephson junctions suitable for digital applications. The key issue to be addressed in this proposal is the applicability of silicon for HTS digital applications.

Fabrication issues

On - chip uniformity and reproducibility - Based on our present experience with the e-beam junctions, we are reasonably confident that uniformity and reproducibility will not be a problem. Nevertheless, they should be addressed and evaluated in the context of a multi-junction technology on silicon substrates. The main issues of importance are:

- uniformity of the initial HTS film;
- I_c, R_n, and I_cR_n product spreads on a chip
- run-to-run reproducibility for various writing conditions;
- uniformity after the stabilizing annealing

II.1.2. RSFQ Circuits

We will use the e-beam junctions to implement simple digital circuits of the RSFQ family, which use single quanta of magnetic flux to code digital bits.[7] Theoretical estimates and experiments with LTS (Nb trilayer) circuits of this kind indicate that this family can be used for ultra-fast processing of digital information, with very low power consumption, dc power supply, and convenient option of self-timing. These features make the RSFQ technology very promising for several application niches in instrumentation, radars, communications, and high-performance computing.[7] The first attempts to implement the simplest HTS RSFQ circuits were, however, either not conclusive[9] or confined to helium temperatures due to use of a LTS ground plane.[10]

We believe that the major challenge here is a necessity of quantitative circuit design (which was lacking is the previous work[11,12]). In fact, due to operation at higher temperatures the HTS RSFQ circuits should use Josephson junctions with proportionally higher critical currents to avoid thermally activated errors. Higher currents imply lower inductances ($L \propto \Phi_0 / I_c \propto T^{-1}$) which may have to decrease

to the values below 1 pH in some cases. Present-day HTS integrated circuit technologies are still confined to 1 - 2 superconducting layers, making reduction of the inductances and their calculation for a given layout a very complex task involving 2D and 3D magnetic field modeling.

II.1.3. HTS Thin Films on Silicon:

The "conventional" HTS compatible metal oxide substrates such as $SrTiO_3$ and $LaAlO_3$ are problematic for high frequency applications. Large epitaxial quality metal-oxide wafers are typically expensive and difficult to acquire. The dielectric constants of these materials tend to be large (e_r between 25 and 1000), lossy, with strong temperature dependence and substantial sample to sample variability. The electronic properties and defects of these substrate materials are quite poorly understood. These factors make it extremely difficult to develop high performance HTS components, and these difficulties will translate at best into higher cost and lower yields in a manufacturing environment. High quality Josephson junctions have so far only been achieved on a handful of expensive, lossy and mechanically fragile oxide materials (the previously mentioned $LaAlO_3$, $SrTiO_3$ and related perovskites being the most notably

The absence of an inexpensive substrate material good high frequency properties and a compatible HTS Josephson junction technology is a serious obstacle for high speed digital applications of Josephson junctions.

The most promising substrate material for integrating HTS and semiconducting devices is silicon. A process for growing high quality epitaxial HTS films on buffer layers on silicon has been developed[13,14] and is utilized routinely at Advanced Fuel Research for its work in bolometric infrared detectors. A facility for growth of the HTS films on Si wafers, originally developed at *Xerox* PARC[13], was established at *AFR, Inc.* in early 1991. The method used is the technique called pulsed-laser deposition (PLD). Our work centers on the most common electronic thin-film HTS-application material: $YBa_2Cu_3O_{(7-d)}$ or YBCO. Silicon wafers and Si compounds react chemically with YBCO at film growth temperatures[15], so a buffer layer of yttria-stabilized zirconia (YSZ) is first grown epitaxially on the Si wafer surface. Preparation of the fresh Si surface must also be included in the process, since all Si surfaces are coated with a native oxide that typically degrades epitaxy unless it is removed by chemical or thermal treatment.[13,16] The facility depicted in Figure 7, epitaxial YBCO films on the YSZ-buffered Si (i.e., $J_c \sim 3 \times 10^6$ A/cm^2).

II.2 Task 1 - Josephson Junction Fabrication and Testing

There were three areas of activity in this Task: 1) improvements to the Pulsed Laser Deposition (PLD) facility to achieve HTS films suitable for junctions, 2) patterning and testing the films and junctions, and 3) developing methods for overcoming films stresses so that thick films can be formed.

II.2.1 Improvements to the PLD Facility

During the course of fabricating working junctions and SQUIDs from thin YBCO films fabricated on silicon substrates, it was observed that the junctions were not well matched in critical temperatures. This non-uniformity was primarily attributed to non-uniformities within the films. To improve the film uniformity, and to accomodate the demands of other projects, we built a new substrate heater for the deposition system to provide more uniform temperatures over larger substrate areas. The new heater was built to allow deposition onto 12 mm square chips, which can subsequently be diced into four 5-mm square chips. With this arrangement, it is possible to fabricate and test many more junctions from a single deposition and gather more and better statistics on junction properties.

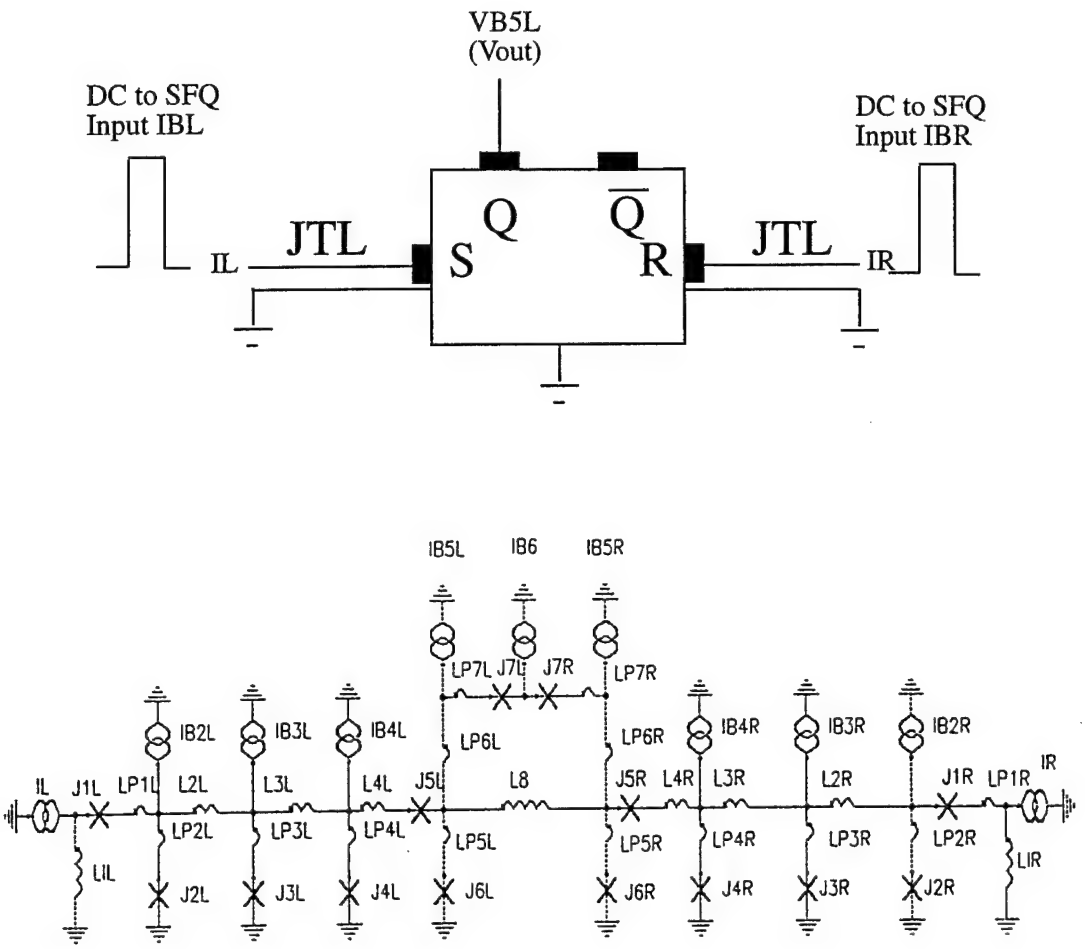

Figure 5 Equivalent circuit of an RSFQ structure comprising two input DC/SFQ converters, two JTLs, RS flip-flop and output SFQ/DC converter.

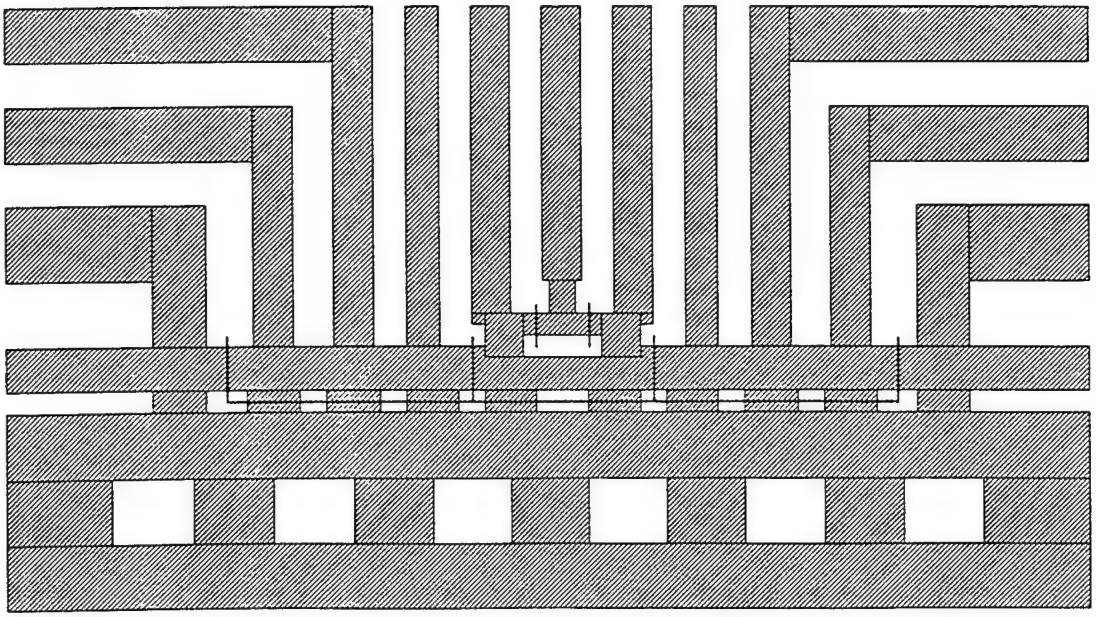

Figure 6 Single-layer layout of the RSFQ circuit shown in Figure 5. Minimum line width is 2 μm. Solid lines across the bridge denote e-beam junctions successful)

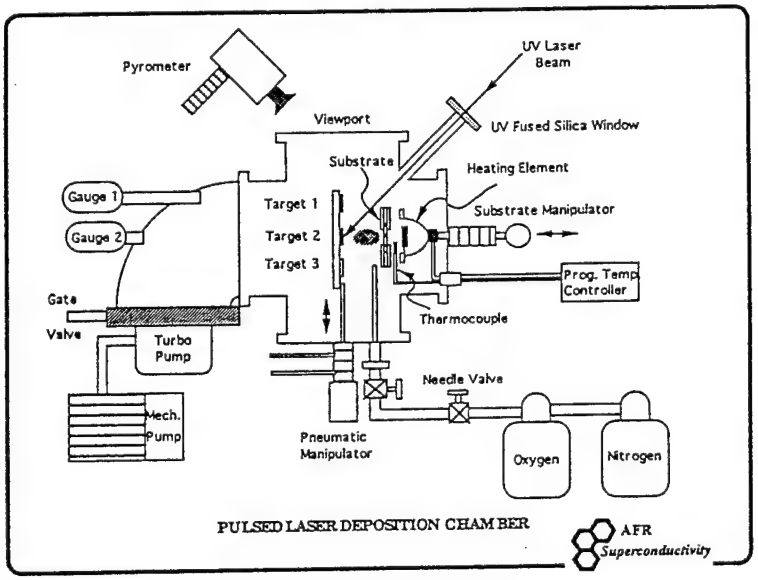

Figure 7 Schematic view of the AFR pulsed laser deposition system.

Two films of YSZ buffered YBCO films were grown on silicon substrates and sent to Professor Gurvitch's laboratory at SUNY at Stony Brook. The films were tested for resistance vs temperature (see Figure 8) and displayed excellent (< 2 K) transition widths. Work there is currently underway at Stony Brook to fabricate Josephson junctions.

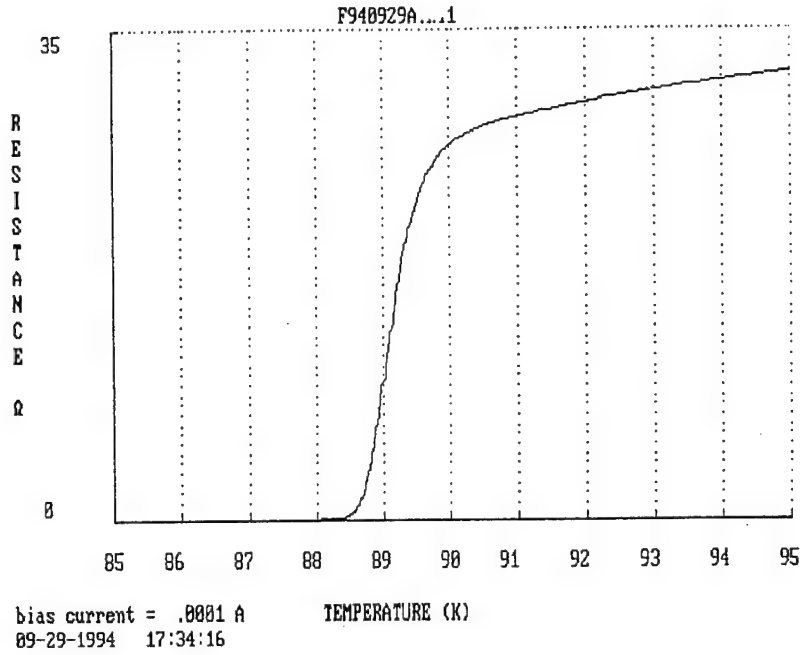

Figure 8 R vs T of YBCO Film to be processed into junctions.

The film had good superconducting qualities as determined by resistance Vs. temperature measurements at AFR and was shipped to Stony Brook for junction fabrication. The film was etched into three bridges approximately four microns across and measured again for resistance vs temperature Unfortunately, the no supercurrents were detected. Two of the junctions were highly resistive at all temperatures, and the third showed a partial transition at 90 K, but retained a residual resistance of 400 Ω below the superconducting transition temperature of the film. The R vs T for the bridge is shown in Figure 9.

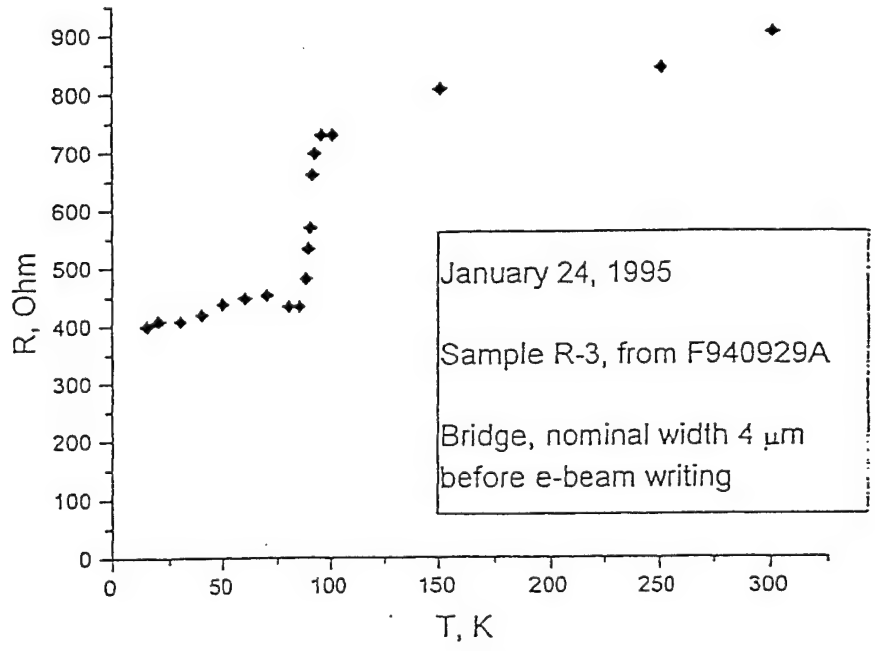

Figure 9 R Vs curve for a microbridge patterned from a YBCO film on YSZ buffered silicon

The rest of the unpatterned film was remeasured using silver paste dots as contacts to determine if the entire film was bad. We found that the film was still superconducting with a T_c of 89 °C. From this we conclude that either the patterning process damaged the bridges, or that the film was sufficiently non-uniform that the bridge was traversed by some completely non-superconducting regions or grain-boundaries.

In order to demonstrate that the process was viable, we processed and earlier film of YBCO on YSZ-buffered silicon into working Josephson junctions in April of 1994. The Josephson behavior of this device was established by measuring microwave induced Shapiro steps, magnetic modulation of the critical current. These results are shown in Figures 10 and 11.

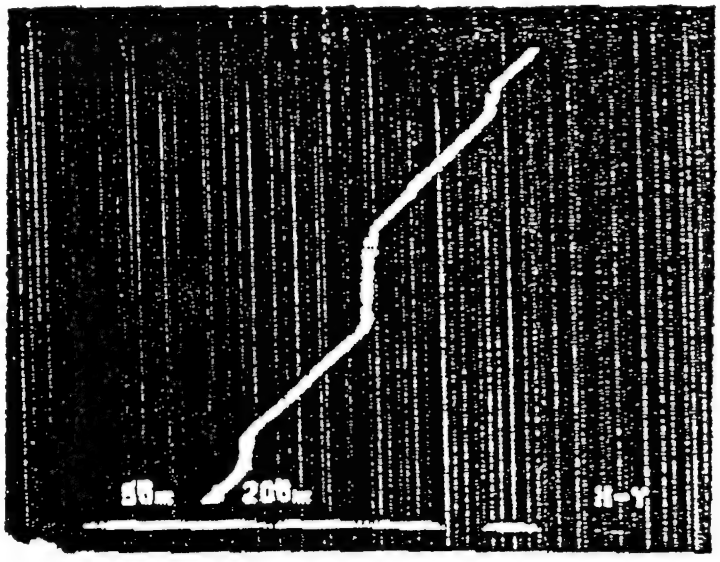

Figure 10 Microwave induced Shapiro steps in the current voltage characteristic of an E-beam modified Josephson junction fabricated from YBCO on YSZ buffered silicon. The data were measured at 52 K.

A new film of YBCO on YSZ-buffered silicon prepared with the improved PLD system was fabricated into working Josephson junctions and a SQUID.

Two SQUID's were fabricated. SQUID R1 did not exhibit any magnetic field modulation, although the shape of the current-voltage (IV) characteristic was RSJ-like. This SQUID exhibited clear microwave induced Shapiro steps in the IV curve. Figure 12 shows the dc IV curve of this SQUID. Figure 13 shows Shapiro steps in the IV curve of SQUID R1 (at 54 K) as induced by a 10.2 GHz microwave source. This SQUID had a resistance of approximately 0.4 s.

SQUID R1 was fabricated by e-beam modification using a beam dwell time of 600 ms, and 2048 dwell points. These conditions usually give T_c of ~50 K, but in this case, T_c for the SQUID was ~61 K. This is probably due to inhomogeneity in the film, which could result in significantly different critical temperatures between the two junctions of the SQUID. If one of the junctions was completely non-superconducting, then we would expect the structure to display the observed behavior.

SQUID R2 showed both SQUID-like magnetic interference and microwave induced steps in the IV curve. Figure 14 shows an SEM image of this SQUID. Figure 15 shows the dc IV curve for this device at a temperature of 40 K. Figure 16 shows the IV curve under the influence of 10.2 GHz microwaves. Note the existence of pronounced Shapiro steps. Figure 17 shows the magnetic interference pattern of SQUID R2.

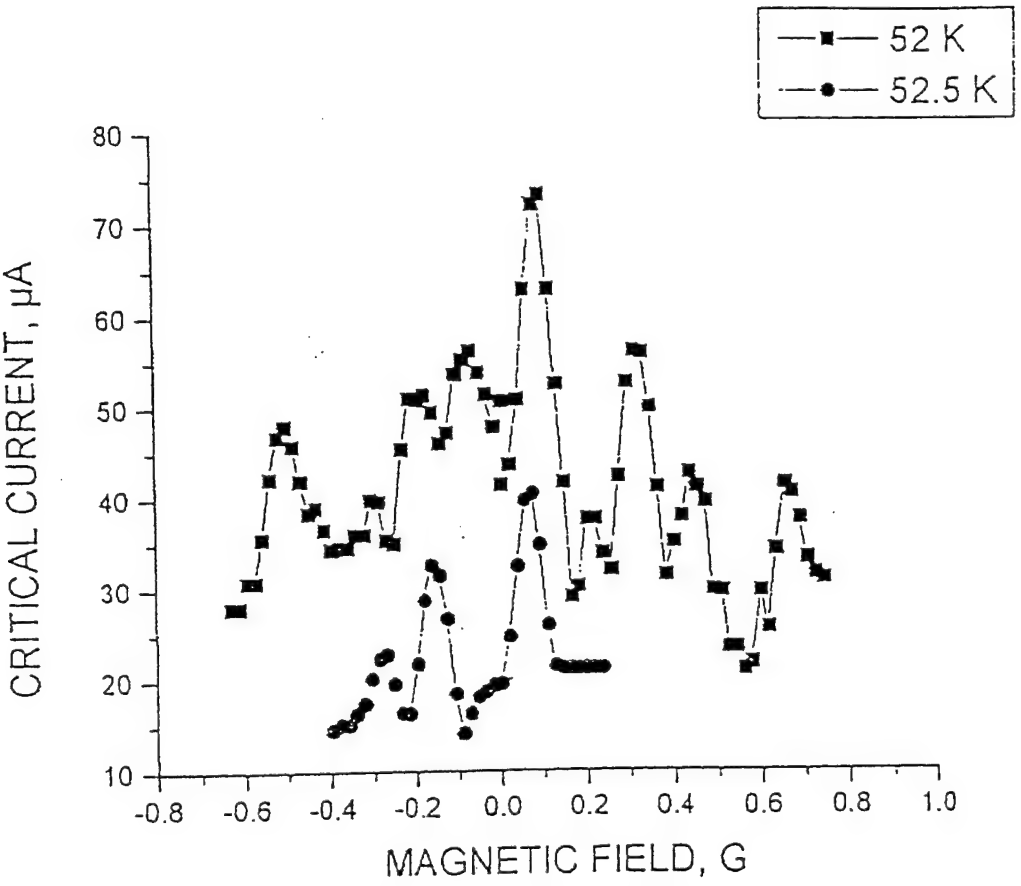

Figure 11 Magnetic field dependence of the critical current fo an E-beam modified Josephson junction fabricated from YBCO on YSZ buffered silicon.

II.2.2. Compliant Buffer Layers

During the course of studying the various parameters which impact the performance of RSFQ devices in Task II, we identified excess parasitic inductance as a significant hurdle for RSFQ fabrication. The dominant contribution to parasitic inductance is the kinetic inductance. This scales inversely with thickness, so it is advantageous to be able to grow thicker films. This is, however, a problem for YBCO films on silicon. The different thermal expansion coefficients of the HTS thin film and the silicon substrate results in the accumulation of tensile strain in the film during cooldown. This causes cracking for films thicker than about 70 nm. A method to deposit thicker films on silicon would be highly desireable, particularly if it did not require the use of buffer layers with inordinately high dielectric constants. We are developing a new type of buffer layer that can relieve strain between film and substrate by plastic deformation. This development, if successful will be a significant breakthrough for HTS on Silicon technology by essentially eliminating both stress induced cracking and parasitic kinetic inductance. The buffer layer consists of a thin film of a soft glass situated between the silicon substrate and the YSZ/YBCO bilayer. The soft glass film will be chosen to have a strain annealing temperature well below the growth temperature. The structure is shown in Figure 18. The fabrication of the buffer layer will involve the processes of film deposition and wafer bonding. During cooldown, as the film cools down, the HTS and YSZ layers can contract faster than the substrate, and the glass film will accomodate the strain by deforming viscously, until the substrates cool below the glass strain point.

Near the end of this Phase I research, we began preliminary work to fabricate this compliant buffer layer on a silicon substrate. We obtained silicon wafers coated with boron-phosphorus-

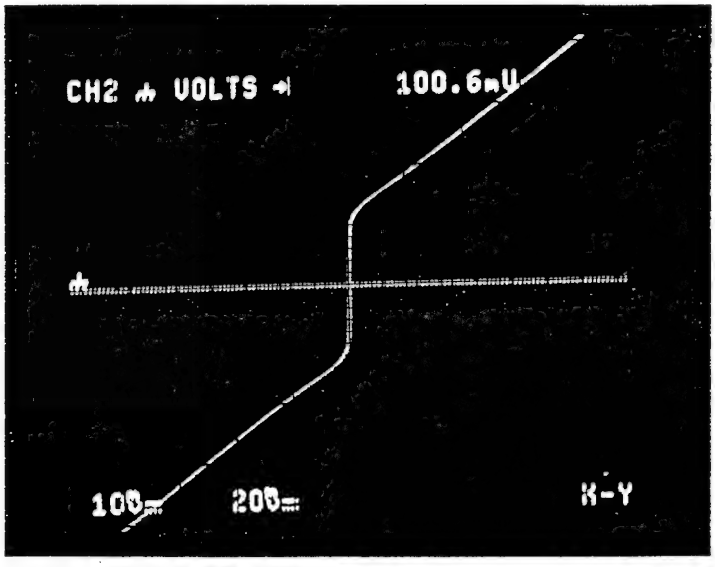

Figure 12 Current-Voltage characteristic of SQUID R1 at a temperature of 61 K.

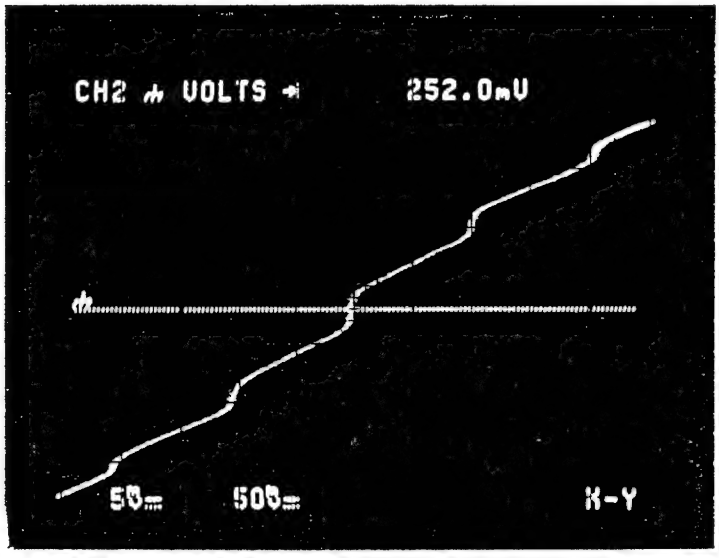

Figure 13 Microwave induced steps in the current voltage characteristic of SQUID R1 at a temperature of 54 K.

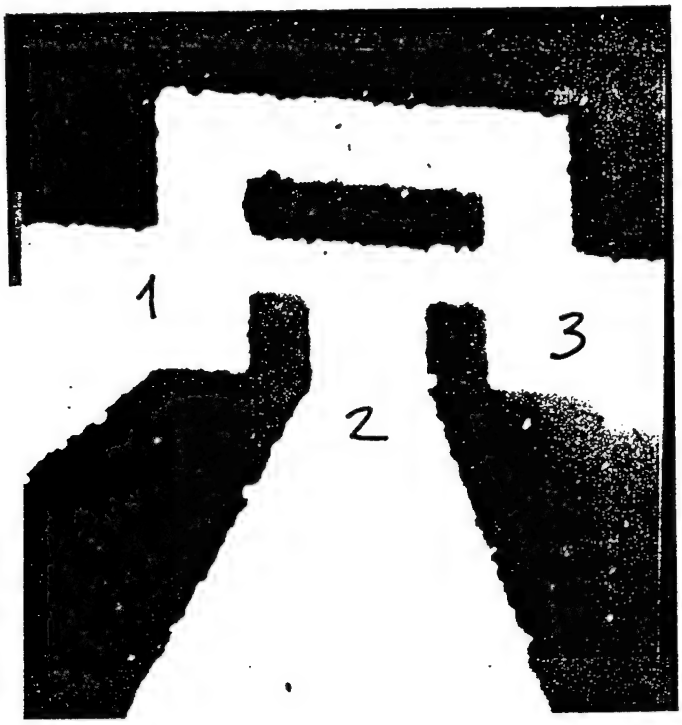

Figure 14 SEM micrograph of SQUID R2.

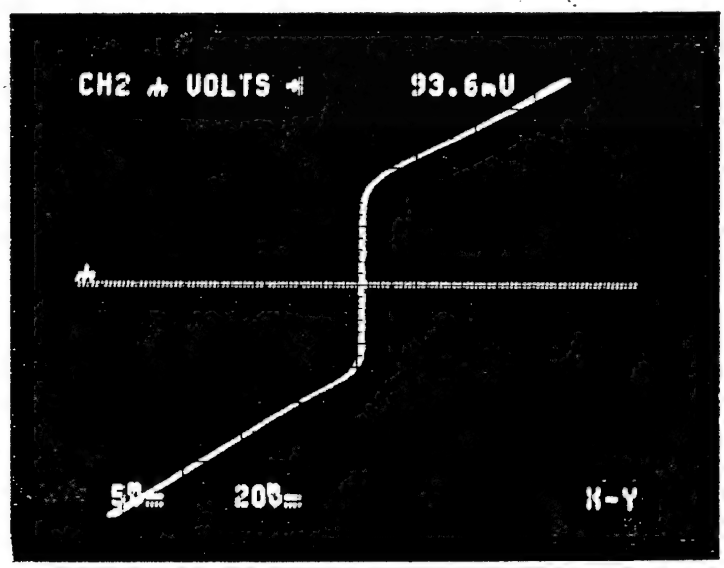

Figure 15 DC IV curve of SQUID R2 at a temperature of 40 K.

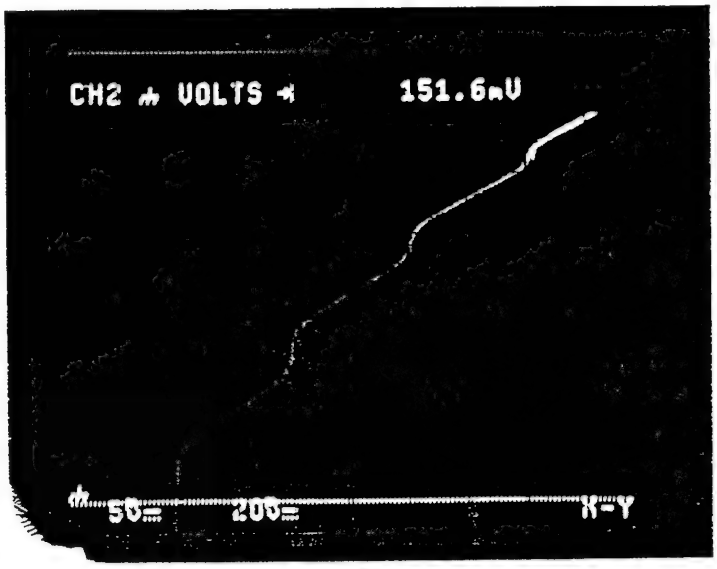

Figure 16 IV curve of SQUID R2 at T = 39 K, under the influence of 10.2 GHz microwaves.

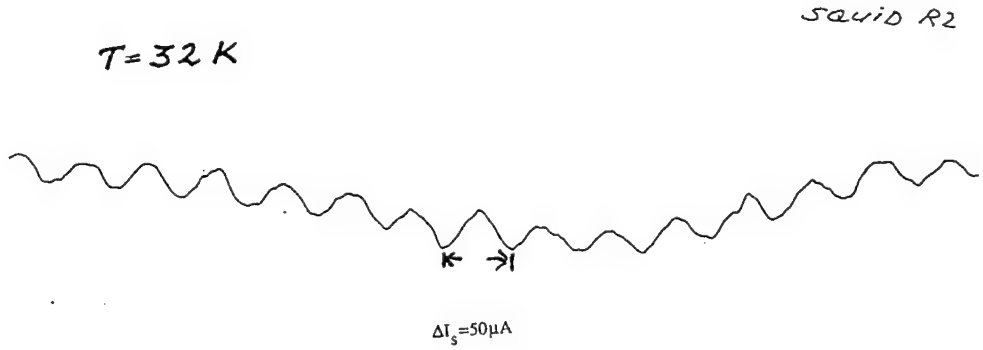

Figure 17 Magnetic interference pattern of SQUID R2 at 32 K.

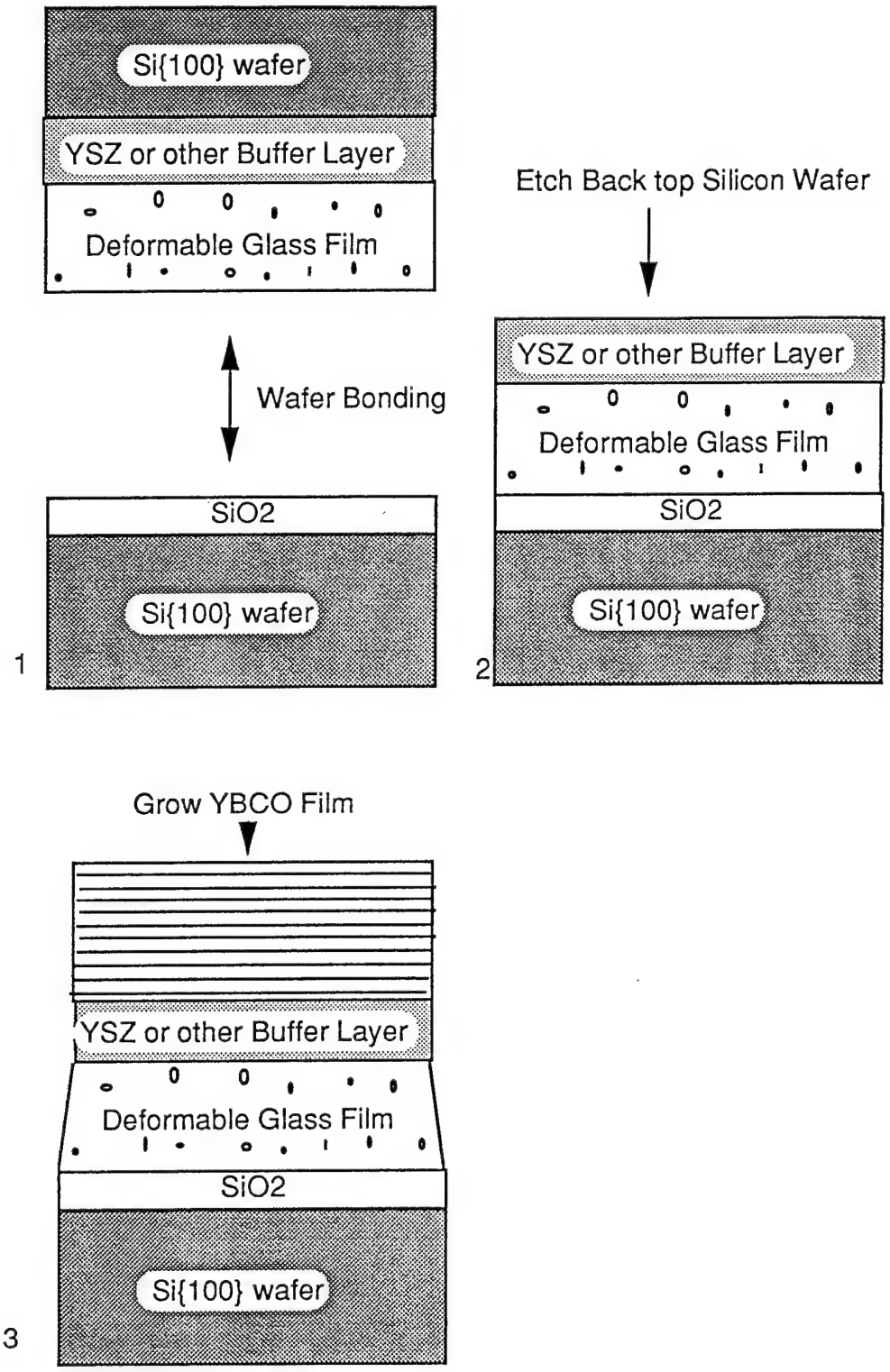

Figure 18 Schematic of plastic buffer layer fabrication process. After growth, deformable glass buffer film layer relieves strain of thermal expansion mismatch by plastic deformation.

silica glass with a strain annealing temperature around 500°C, and constructed a low cost wafer-bonding facility. This facility consists of two small vented acrylic cabinets for manipulating and cleaning samples. The work area is curtained off with polyethylene plastic, and maintained at positive pressure with a filtered blower. Initial efforts to bond two Si wafers together were successful. The process followed was to clean the wafers with conventional techniques to strip the native oxide, followed by formation of a new oxide layer, which provides a hydrophilic surface. These wafers are put together wet, and then dried for 24 hours, followed by a 1-2 hour anneal at 700°C. This bonded structure seems to be well bonded, and indicates that our facilities are sufficiently clean and dust-free.

We next applied this technique to bonding a BPSG (boro-phosphate-silicate glass) coated Si wafer to a SIMOX wafer (Si wafer with a buried oxide layer). The BPSG coating is the desired compliant material, and the buried oxide will serve as an etch stop for removing the Si. This resulted in an Si substrate wafer with a BPSG-Si-SiO_2 layer on top. We were able to achieve a good mechanical bond between the two wafers, but the etching process to remove the Si were unsuccessful due to lack of a sufficiently good way to protect the BPSG wafer.

A third experiment used a BPSG-coated Si wafer bonded to a YSZ coated Si wafer. Again, a good mechanical bond was obtained, and again the attempt to etch the Si on the YSZ failed. The goal was to provide a Si substrate with the compliant BPSG layer overcoated with the YSZ. This, then, would be the desired substrate on which to grow the thick films of YBCO. We feel confident that refinements in the etching procedures will allow this technique to be successful in Phase II.

II.3 Task 2- RSFQ Modeling and Design

Early in the program, we identified parasitic inductance as a critical parameter governing the margins and performance of HTS RSFQ devices. Thermal expansion mismatch induced stress limits the overall thickness of HTS films on silicon substrates to under 70 nm. Because this thickness is less than the london penetration depth, typically 150 nm - 400 nm, we expected a substantial kinetic inductance to be associated with wiring and transmission lines. The kinetic inductance associated with the Josephson junctions themselves is still poorly understood.

Because of the importance of inductance to overall circuit performance, we fabricated and measured (Task 3) some dc SQUIDs and RSFQ flip flops incorporating SQUIDs.

The estimated sheet parasitic kinetic inductance is given by the formula $L_{sq}=\lambda_L^2/d$, where λ_L is the London penetration depth, d is the film thickness ($d<<\lambda_L$) and the current distribution is assumed to be uniform. The total loop inductance in a dc squid can be extracted from the magnitude of the magnetic field induced critical current modulation. We performed measurements on a SQUID fabricated from a 25 nm thick film grown on an $LaAlO_3$ substrate by the barium fluoride process. The inductance calculated over a wide temperature range are plotted in Figure 19. Similar results for a much smaller SQUID imbedded in an RSFQ flip flop are also shown in the figure.

The temperature dependence to the sheet inductance is a signature of substantial kinetic inductance. Since kinetic inductance negatively impacts circuit performance, it is essential that careful quantitative account of all sources of inductance be included in circuit design efforts.

The results indicated that kinetic inductance would be a significant hurdle to the success of HTS RSFQ devices, but that, at least for the purposes of Phase I, the inductance was low enough to proceed, and as discussed in Task I, we developed methods to allow the fabrication of thicker films in Phase II.

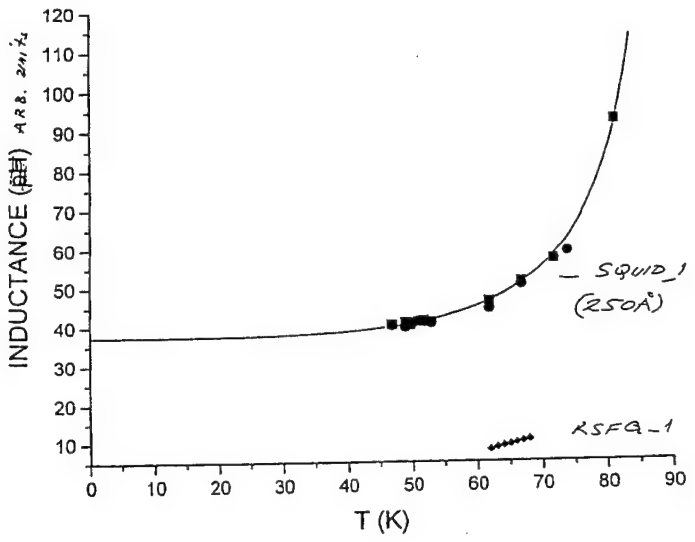

Figure 19. Temperature dependent SQUID inductance for two devices.(AB)

Based on these preliminary measurements and analysis, a more detailed analysis of kinetic inductance was pursued. All RSFQ logic elements depend on maintaining a balance between the Josephson inductance and the SQUID loop inductance such that $2\pi I_c L \approx \phi_0$, where $\phi_0 = h/2e$ is the elementary flux quantum. ϕ_0 is equal to 2.07 mA-pH in practical electrical units. The exact relation between I_C and L is determined by design simulations of a particular logic gate. To ensure that thermal fluctuations do not cause bit errors, the thermal energy unit K_BT must be small compared to the energy scale of the Josephson junction, which is given by $E_J = \phi_0 I_C/2\pi$. Setting $K_BT = 10\ E_J$, we get the result that thermal fluctuations limit the minimum critical current I_c to be at least 38 μA at 90 K. In order that the inductance's can effectively store and process single flux quanta properly, the SQUID inductance is therefore required to be at most $L = \phi_0/(2\pi\ I_C) = 8.6$ pH. Typical inductance numbers for coplanar transmission lines are of the order of 0.5 pH per micron. This implies that careful device design simulations and circuit layout will be required for success. Achieving control over the inductance requires that proper account be taken of all sources of inductance in the SQUID. For this reason, the analysis of the above SQUID results was continued. Assuming that the SQUID modulation depth is entirely due to inductance and not critical current nonuniformity, we found that the low temperature London penetration depth $\lambda_L(0)$ was 370 nm. This is approximately two times higher than what is expected for high quality films. The results under discussion were obtained from films grown by the post-annealed barium fluoride process. It is not surprising that these post-annealed films were of lower quality than films grown in-situ by pulsed laser. If our films on silicon are comparable to PLD grown films on oxide substrates, then we should see approximately a two-fold decrease in penetration depth and a concommittant four-fold decrease in parasitic inductance. If this is born out, then we expect that functional RSFQ logic elements will be possible even with films as thin as 60 nm.

Parasitic inductance - Very thin film transmission lines have two components to the inductance. First, is the more familiar geometric inductance, which arises from the energy stored in the magnetic fields surrounding and penetrating the conductors. Second, is the kinetic inductance, which is often considered a parasitic quantity. The kinetic inductance arises from the kinetic energy of the current carrying cooper pairs. For very thin films, the sheet kinetic inductance is given by $\mu\lambda_L^2/t$ where λ_L is the London penetration depth and t is the film thickness. Using 370 nm for λ_L at low temperatures and t = 5.70 nm we have a parasitic kinetic inductance of 3pH/□ at low temperatures. As T approaches T_C, the London penetration depth diverges, and the parasitic inductance increases as well.

All this implies that thicker films are more desirable from an inductance point of view, and that methods to allow thicker films on silicon would be extremely helpful. At present, film stress provides the main limitation to film thickness. This is one of the reasons why we are examining the roles of new buffer layers in reducing film stress.

SQUID R2, discussed under Task 2 (Figure 17), exhibited magnetic modulation of the critical current only at temperatures at least 7 K below the critical temperature of the SQUID. This suggests that one of the junction had a higher T_c of 45 K, and the other had a T_c around 37 K. The magnetic modulation was measured by injecting current across the SQUID loop, between terminals one and three as shown in Figure 14. For this geometry, the inductance is given by $L=\phi_o/\Delta I_s$, where ΔI_s is current amplitude associated with one oscillation of the SQUID. From the measurement shown in Figure 17, we infer that the inductance is approximately 40 pH. This value is approximately a factor of two higher than is typically seen with SQUID's fabricated on conventional i.e. $LaA1O_3$ substrates. This difference in inductance is likely due to parasitic kinetic inductance associated either an increased magnetic penetration depth, or possible to microstructural defects in the film used for the SQUID.

II.4. Task 3 - RSFQ Circuit Fabrication and Testing

In order to proceed with this Task in parallel with Tasks I and II, we fabricated dc SQUIDs and an RSFQ flip flop incorporating several SQUID's made using the AT&T barium fluoride process on $LaAlO_3$ substrates. The YBCO films were 25 nm thick. The magnetic field dependence of the critical currents and the modulation depth as a function of bias and temperature were measured. Figure 20 shows the current modulation depth as a function of bias voltage for a SQUID imbedded in an RSFQ flip flop at 66 K. The measurements show nearly a 50% modulation in current at low bias voltages, an encouraging result.

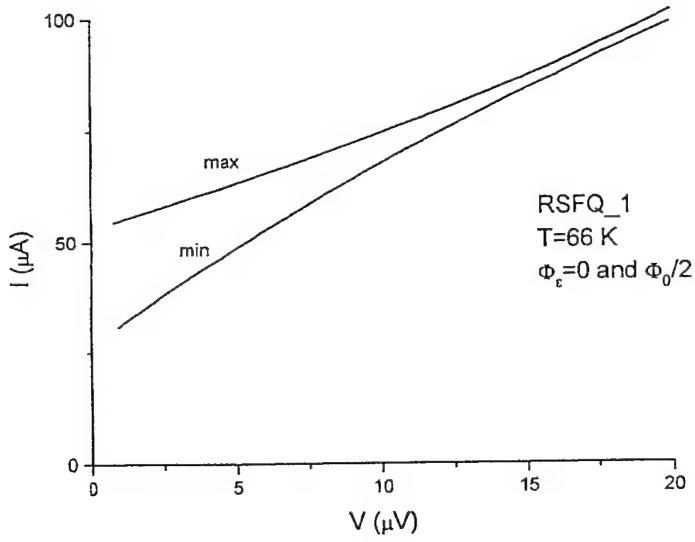

Figure 20 Measured modulation depth of a thin film HTS SQUID in an RSFQ logic element. (AB-2)

Based on the results obtained from this film, a working RSFQ circuit with 14 junctions was successfully fabricated and tested, using a YBCO film grown on a lanthanum aluminate ($LaAlO_3$) substrate. This result is significant because it demonstrates that:

1) the junction technology is sufficiently controllable to manufacture circuits with a significant number of junctions (14 junctions),

2) The circuit design was correct and the film and junction properties e.g. kinetic inductance and critical currents, were within the specified operating margins for successful circuit operation.

3) Correct pulse driven RSFQ logic operation can be successfully verified through dc testing.

The details of this circuit, its preparation and its operation follow:

Direct e-beam writing technique (DEW) was used for preparation of an RSFQ RS Flip-Flop on YBCO thin film operating at 26K.

The most important unique features of the DEW technique instrumental for successful operation of RSFQ circuits are:

1) tunability of the critical temperature T_c (and hence the critical current I_c at an operating temperature).

2) simplicity of the in-plane two-dimensional design combined with the freedom in the arrangement of the junctions.

Technology

Layout of the circuit under investigation was shown in Figure 6. It was made of 500 Å YBCO film deposited on $LaA1O_3$ at AT@T Bell Labs by Shang Hou. After the deposition the wafer was diced into 5x5 mm chips, which were then used for patterning. The patterning was done by standard optical lithography with PMMA resist. YBCO film was wet-etched in diluted HNO_3. Figure 21 shows the final pattern with the minimal feature of 2 μm. Then the junctions were made by DEW in the places shown in Figure 6 as straight lines across the bridges. Electron beam of CM-12 Philips Electron Microscope was scanned once across a bridge to form a weak link. The parameters of the beam were as follows: energy E=120 keV, probe size 35 Å, beam current 5 nA. T_c of the junctions after writing was approximately 35 K.

Operation of the RSFQ RS Flip-Flop

Figure 5 shows the equivalent circuit of the RS Flip-Flop used in the experiment. Below we give a brief description of how it works and then demonstrate its operation at 26 K.

The circuit has a left-right symmetry and consists of four main parts (see Figures 5 and 6).

1. DC/SFQ converter (J1, J2). Current IL opens J2. As a result the fluxoid starts moving to the right by the driving current I2 and antifluxoid to the left. The latter is trapped in the first hole and then comes out of the circuit through J1 when IL is decreased.

2. Transmission line. The fluxoid keeps moving along the transmission line through the junctions J3 and J4 by the driving currents I3 and I4.

3. RS Flip-Flop. (The main cell of the device). Finally the fluxoid gets into the loop J6L, J6R and stays there in the absence of a driving force.

4. SFQ/DC converter (J7L and J7R). It serves as an output of the Flip-Flop. It detects the flux in the lower loop cell. State "1" corresponds to the state when one fluxoid is trapped in the

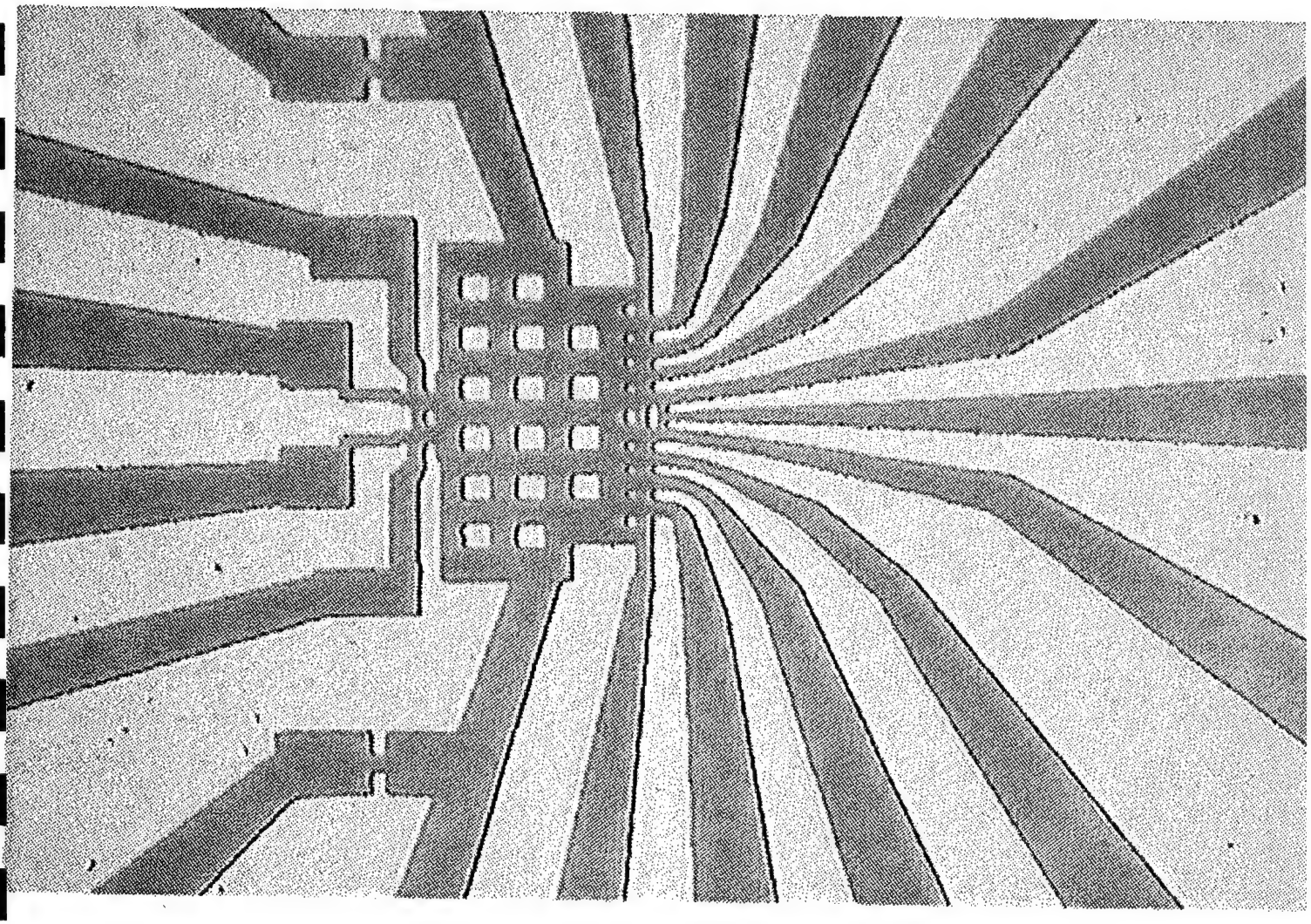

Figure 21. Optical Photograph of the RSFQ Flip-Flop.

lower loop which results in the corresponding voltage in the upper SQUID when it is biased by some current higher than its critical current. State "0" corresponds to the absence of a fluxoid in the lower cell. This is achieved by applying current IR to the right part of the device. It generates an antifluxoid which moves to the left and annihilates with the previously trapped fluxoid in the main cell. If IL generates the fluxoid and the Flip-Flop is currently in the state "1", junction J5 opens and the fluxoid leaves the circuit without disturbing the state of the Flip-Flop. The same is true for the antifluxoid.

Experimental Setup

The chip was installed on a 24 contact probe and placed in a transport helium dewar. Temperature was stabilized by a Temperature Controller (Lake Shore). Measurements were carried out using an automated testing setup which had been developed at Stony Brook. Its hardware part is an advanced version of the system developed earlier at NIST. The setup consists of three main parts: a cryoprobe with passive LF filters located in a transport dewar, a set of 48 ADCs and 48 DACs, and IMB PC running *Octopus* software. *Octopus* was used for all low-frequency analog and digital experiments with High-T_c RSFQ RS Flip-Flop. *Octopus* is a TCL interpreter extended to have low-level access to the buses and system timer. It can display real-time analog data, acquire I-V curves and perform various kinds of digital testing. One of the elementary operation used for testing the high-Tc RSFQ RS Flip-Flop is sending a test pattern to the tested circuit and verifying its response.

Experimental Data

The experimental procedure for testing the RSFQ RS Flip-Flop was the following.

1. The operating temperature 26 K was chosen so that the critical current of the SQUID was 50 μA. At this critical current the maximum voltage modulation depth was 12 μV.

2. Transmission line was biased by currents I2L(R), I3L(R), I4L(R) equal to 0.1 mA each. This value corresponds to approximately half the value of critical current of each junction in the transmission line.

3. The SFQ/DC converter was biased at 65 μA and magnetic currents IB5L-IB5L were chosen to have maximum voltage difference between state "0" and "1".

4. The current IL was applied and voltage V_{sq} on the SFQ/DC converter was measured while increasing IL. At some value of IL there appeared a jump in V_{sq} (Figure 22a) which corresponds to fluxoid entering the main loop ("record" or "flip"). Stability of state "1" can be checked by once more increasing IL to make sure that there are no other states (Figure 22b).

5. To switch the device from "1" to "0" current IR was applied and at some value there is a jump in V_{sq} from "1" back to "0" state ("erase" or "flop", Figure 22c). Figure 22d shows a proof that the device is still in state "0".

To eliminate direct influence of the currents IL and IR on the SFQ/DC converter and Flip-Flop we applied an additional small differential current between IB5L and IB5R proportional to the currents IL or IR to compensate leakage current from the input. The coefficient of proportionality give us an exact value of the leakage current which was approximately 5% of the input currents IL and IR. This procedure fixes a set point of SFQ/DC converter during all measurements. This fact completely rules out the possibility of switching SQUIDS due to the leakage current.

Operation of the flip-flop is demonstrated in Figure 23. A sequence of digital double current pulses is applied to IL and IR and switches the flip-flop to states "0" and "1" respectively. It can be seen that the first pulse from Il sets the flip-flop ("1") and the second IL pulse does not

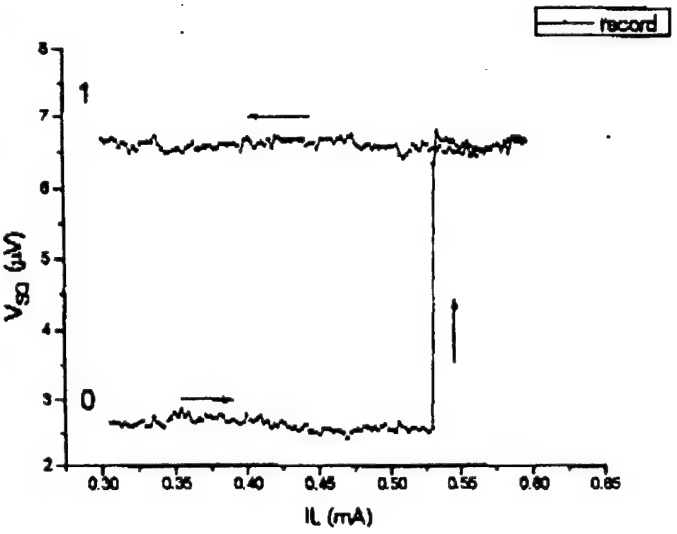

Figure 22a

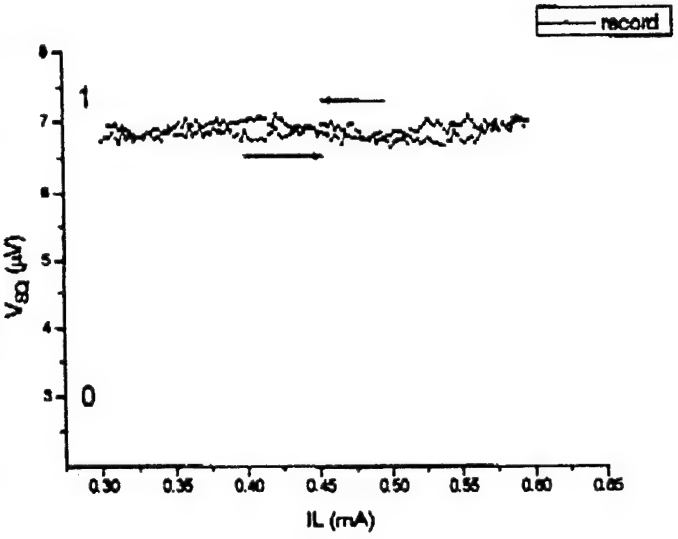

Figure 22b

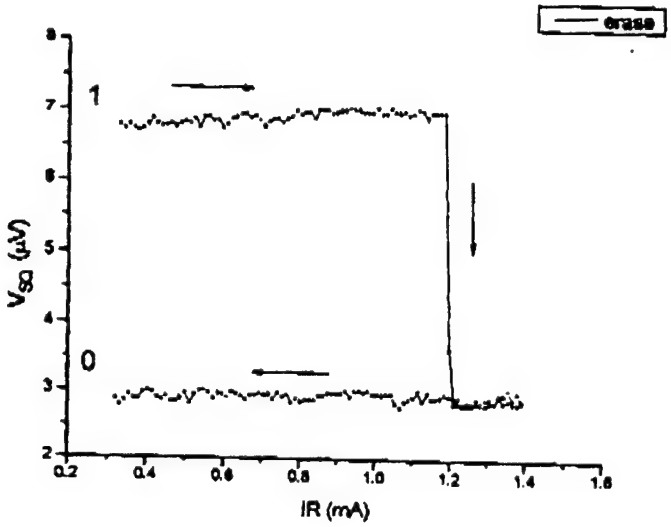

Figure 22c

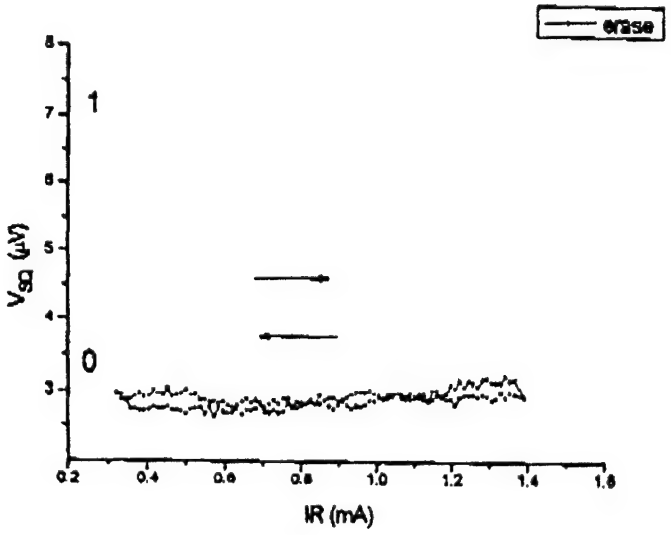

Figure 22d

Figure 22 Measurement of Logic States for RSFQ RS Flip-Flop

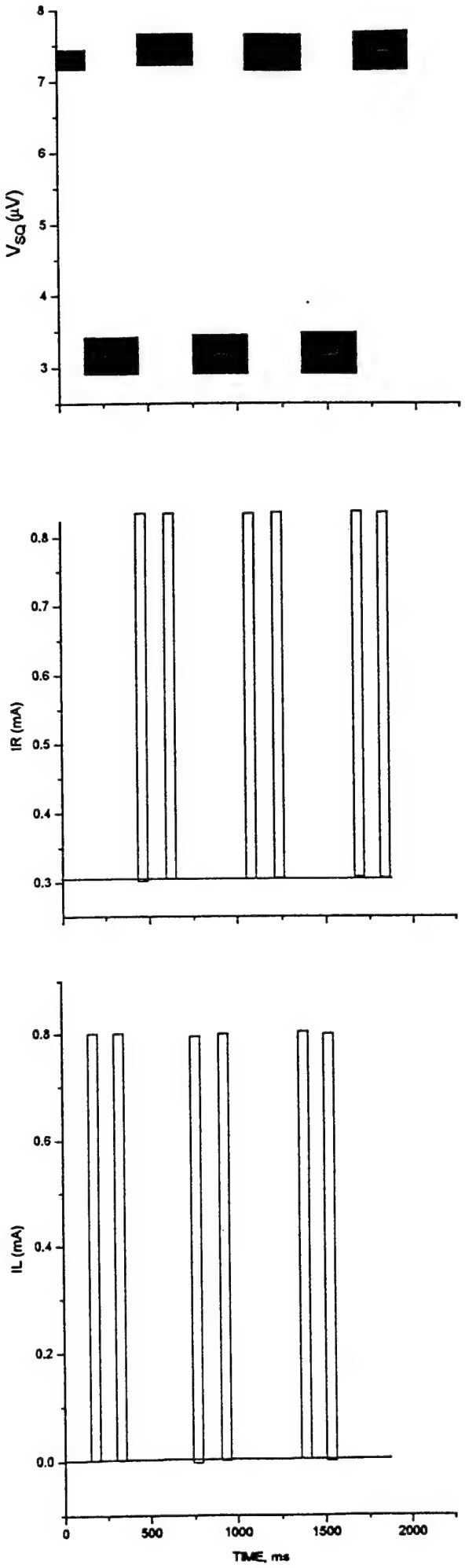

Figure 23 Operation of RSFQ RS Flip-Flop

change the state of the flip-flop. The pulse IR resets the flip-flop ("0"), etc. The noise is characterized by the width of the corresponding voltages V_{sq}.

Additional experiments proved that the device was indeed operating as an RSFQ flip-flop, that the Josephson transmission line inputs circuitry was operating as expected, and that the switching thresholds and statistics were reasonable.

1. Analog data pattern:

The operation of the flip-flop is demonstrated in Figure 24 by applying digital current pulses to IL and IR (IBL and IBR) to switch the flip-flop to state "1" and "0" respectively; analogue voltage signals V_{out} are measured in the main SQUID loop.

Signal/noise ratio corresponding to the readout pulse is approximately 20. The test sequence is as follows. First, a double pulse is applied to IL the s (set) input to the rs flip-flop. The first pulse switches the flip-flop to state "1" (high V_{out}). The second pulse is applied to make sure that this is stable. Next, another pair of pulses is applied to IR (the r or "reset" input). The first pulse resets the flip-flop to the zero state (V_{out} low)as shown in the top trace. The second pulse demonstrates that this state is also stable.

2. Derivatives of the bias currents:

To prove beyond any doubt that the RSFQ works the way it should we conducted another series of experiments. We need to show that DC/SFQ converter operates properly; junction J2 opens and the flux starts moving along the transmission line (through junctions J3 and J4) until it is trapped in the main loop of the device.

In order to do that we measured the change in the values of IBL (IL) and IBR (IR), corresponding to the change in the respecting bias currents IB2L, IB3L, IB4L etc. (partial derivatives). The results are shown in Figure 25. We found that the bias influence is the strongest on the current IB2L, which means that indeed it is this junction that reaches threshold and switches when you apply the current to IL. We obtain the same result for IR as well (for junction J2R). The experimental values of these derivatives do not differ much from the results of the computer simulation (using PSCAN software).

3. Thermal noise distribution of the value of the current IL (IR) (position of the jump).

In order to check the reliability of the device and the influence of the thermal noise we studied a few hundred cycles ("0" - "1"; "1" - "0") and measured the distribution function of the values of IBL (IBR) at which the flip-flop operates. Figure 26 shows the resulsts of 100 cycles. The first conclusion we can come to is that it worked 100 times out of 100.

More importantly the distribution function has the right shape - it is not quite symmetric - and can be very well fitted by a theoretical formula for thermal fluctuations with the mean deviation of IBL approximately 0.010 mA (for this device configuration). The experimental value is approximately 0.015 mA.

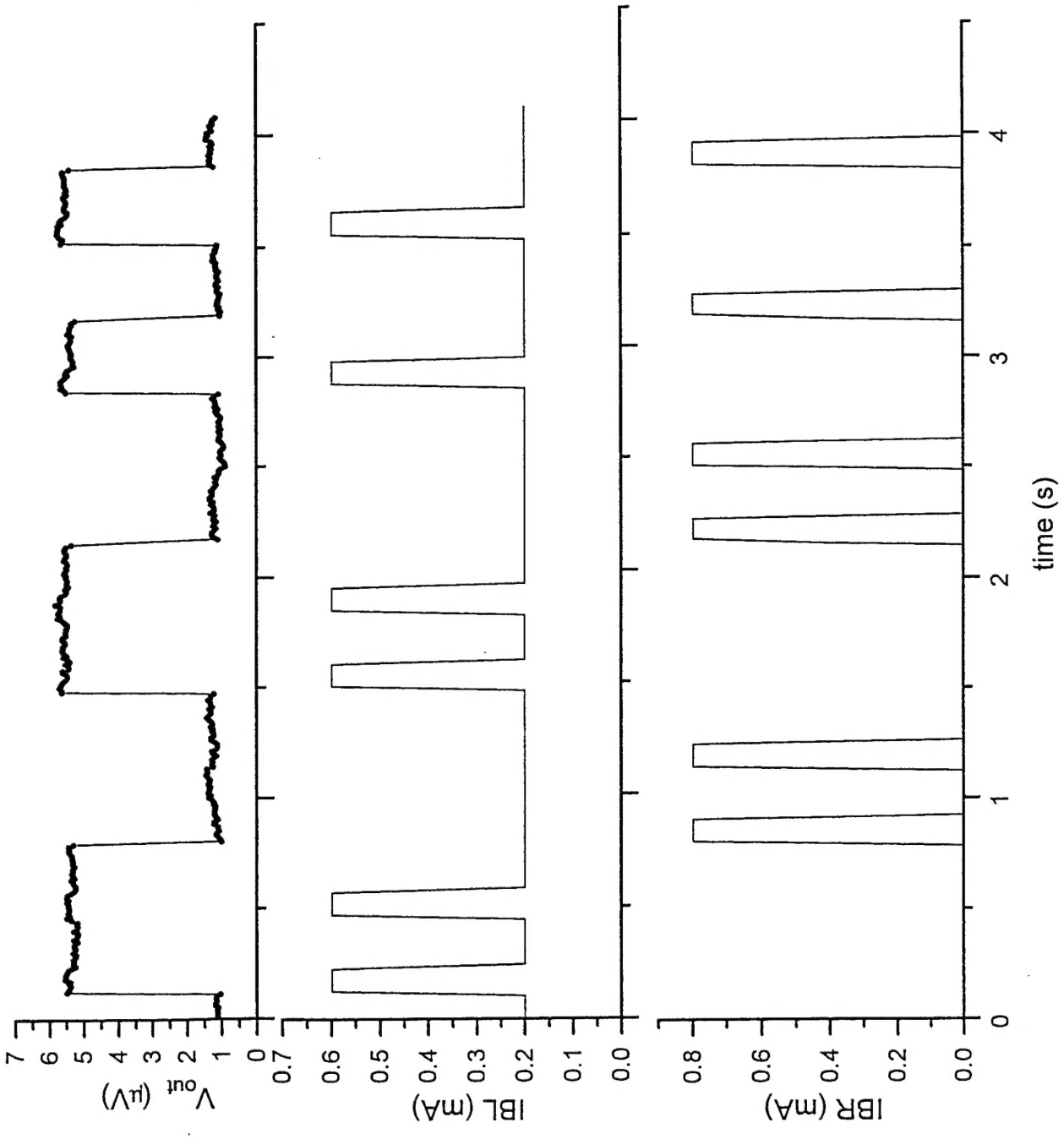

Figure 24 Demonstration of the flip-flop operation. The top trace shows the analogue measurements of the readout SQUID interrogating the flip-flop state. The middle and lower traces show the currents applied to the JTO coupled set and reset inputs.

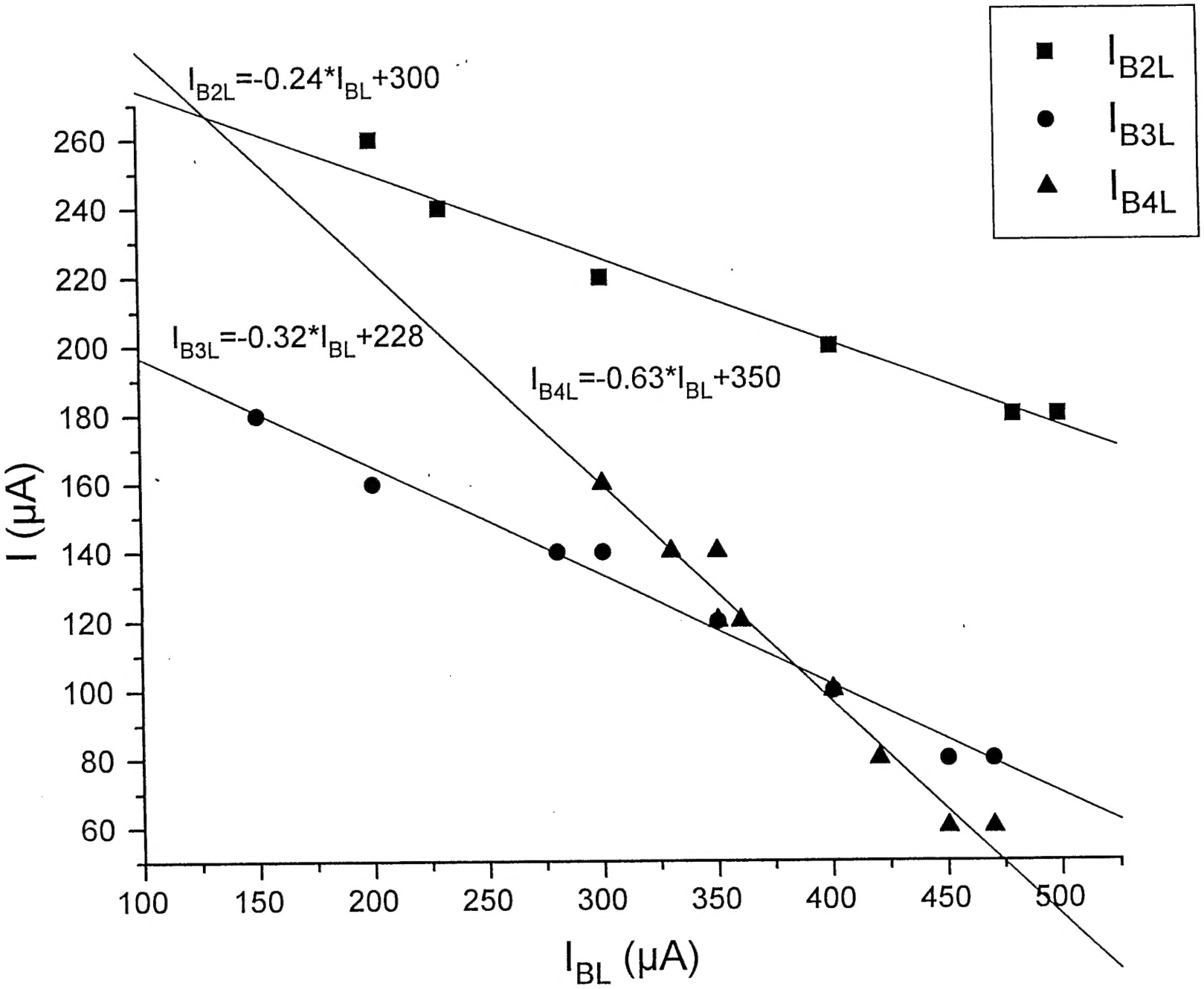

Figure 25 Dependence of the JTL junction bias currents with respect to the input current I_L, showing that the first junction in the JTL will switch first.

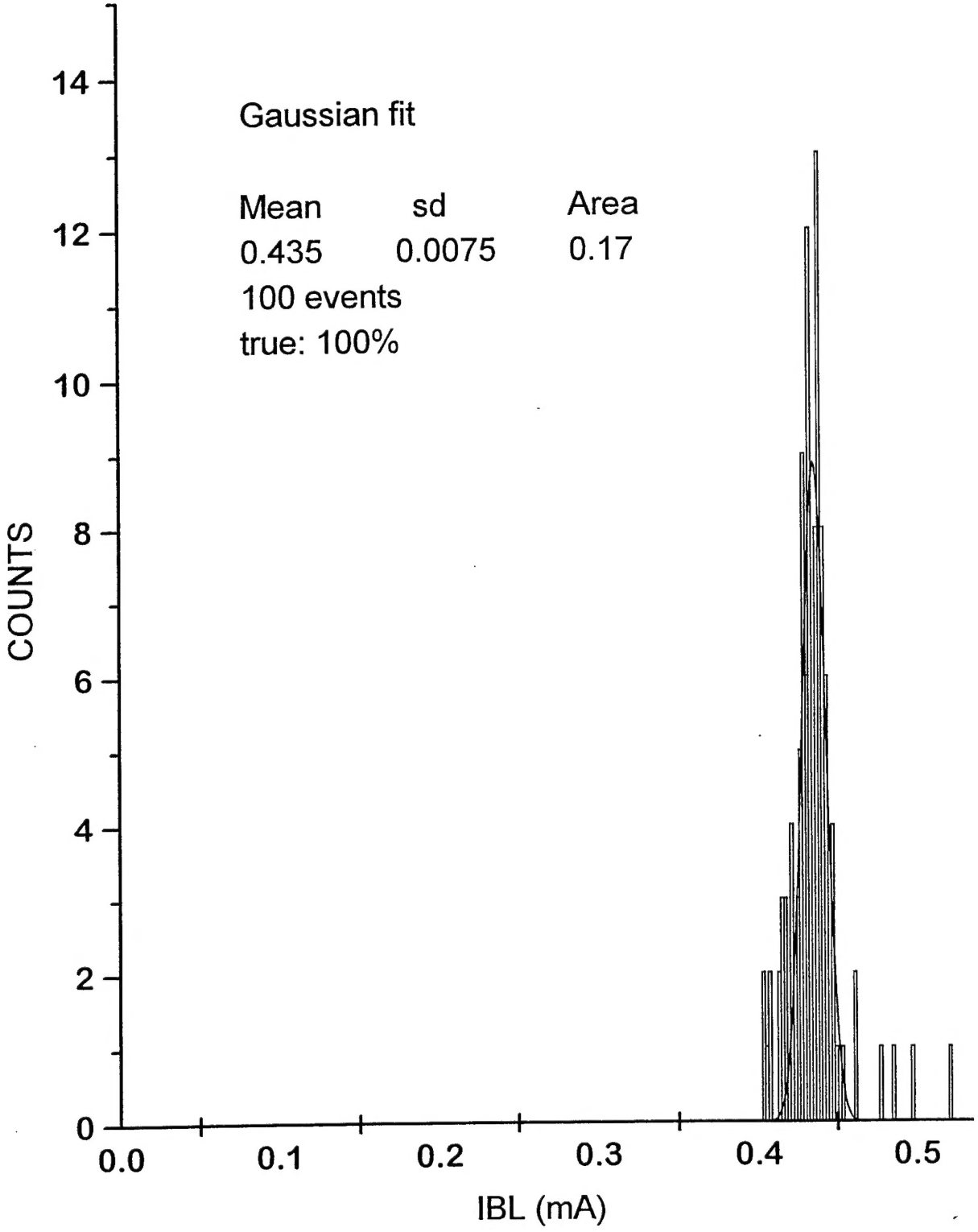

Figure 26 Histogram of switching events vs input current IB_L. Gaussian fit is shown as the solid curve.

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